IN THE CLAIMS

What is claimed is:

| 1 | 1. A circuit to search an external memory containing search results based on a search value |
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| 2 | received from an external controller, comprising: |
| 3 | a hash unit able to generate a hash output based on the search value, wherein said hash |
| 4 | unit is operationally connected to an input bus connecting the circuit to the |
| 5 | external controller; |
| 6 | a CAM unit able to store a CAM database of possible instances of the search values |
| 7 | known to cause hash collisions in said hash unit and able to match the search |
| 8 | value against said CAM database such that a CAM output is provided if a match |
| □ 9 | exists, wherein said CAM unit is also operationally connected to said input bus; |
| 口 9 山 山0 | a logic unit able to: |
| | receive any said CAM output provided and to create an address value based there |
| J12 | on and to provide that said address value on an output bus connecting the |
| 回 过 3 | circuit to the external memory, wherein said address value represents an |
| <u> </u> | address in the external memory; and otherwise |
| 五5 日6 日7 日7 | receive said hash output and to create one or more hash addresses based there on, |
| 급 6 | to receive a hash pointer value and create said address value based there |
| <u> </u> | on, and to receive a hash hit signal and responsive there to provide said |
| 18 | address value on said output bus; |
| 19 | a search data storage able to: |
| 20 | store a plurality of said hash pointer values, wherein said hash pointer values |
| 21 | represent potential instances of said hash addresses; |
| 22 | store a plurality of search data values, wherein said search data values represent |
| 23 | potential instances of the search values; |
| 24 | receive a said hash address from said logic unit and based there on retrieve a said |
| 25 | hash pointer value and provide it to said logic unit; and |
| 26 | retrieve a said search data value based on said hash pointer value; and |
| 27 | a comparator operationally connected to said input bus and able to receive the search |
| 28 | value there from, to receive said search data value from said search data storage, |
| 29 | to compare the search value and said search data value to determine whether a |

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match exists and, if a said match exists, to provide said hash hit signal to said logic unit, thereby permitting the external memory to not store any instances of the search values.

- The circuit of claim 1, wherein said logic unit is further able to generate a search hit signal based on said hash hit signal and whether a said match exists in said CAM unit, and to provide said search hit signal to the external controller via a hit line, thereby confirming that a current instance of the search result.
 - 3. The circuit of claim 1, wherein said hash unit is programmable to employ different hash algorithms.
 - 4. The circuit of claim 3, wherein said hash unit includes a plurality of pre-programmed hash algorithms, thereby permitting selectively employing a particular said hash algorithm.
 - 5. The circuit of claim 1, wherein said CAM unit is programmable with new entries for said CAM database, from the external controller, thereby permitting the external controller to program the circuit to avoid new hash collisions.
 - 6. A circuit for searching an external memory containing search results based on a search value received from an external controller, comprising:

hash means for generating a hash output based on the search value, wherein said hash

means is also for operationally connecting to input bus means for connecting the

circuit to the external controller;

CAM means for storing a CAM database of possible instances of the search values known to cause hash collisions in said hash means and for matching the search value against said CAM database such that a CAM output is provided if a match exists, wherein said CAM means is also for operationally connecting to said input bus means;

logic means for:

| 12 | receiving any said CAM output provided and creating an address value based |
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| 13 | there on and for providing that said address value on output bus means for |
| 14 | operationally connecting the circuit to the external memory, wherein said |
| 15 | address value represents an address in the external memory; and otherwise |
| 16 | receiving said hash output and creating one or more hash addresses based there |
| 17 | on, for receiving a hash pointer value and creating said address value |
| 18 | based there on, and for receiving a hash hit signal and responsive there to |
| 19 | providing said address value on said output bus means; |
| 20 | search data storage means for: |
| 21 | storing a plurality of said hash pointer values, wherein said hash pointer values |
| 22 | represent potential instances of said hash addresses; |
| | storing a plurality of search data values, wherein said search data values represent |
| 24 | potential instances of the search values; |
| -25 | receiving a said hash address from said logic means and based there on retrieving |
| 2 6 | a said hash pointer value and providing it to said logic means; and |
| ⊉ 7 | retrieving a said search data value based on said hash pointer value; and |
| 28 | comparator means for operationally connecting to said input bus means and for receiving |
| 2 9 | the search value there from, for receiving said search data value from said search |
| 30 | data storage means, for comparing the search value and said search data value to |
| 3 1 | determine whether a match exists and, if a said match exists, for providing said |
| 32 | hash hit signal to said logic means, thereby permitting the external memory to not |
| 33 | store any instances of the search values. |
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- 7. The circuit of claim 6, wherein said logic means is further for generating a search hit signal based on said hash hit signal and whether a said match exists in said CAM means, and for providing said search hit signal to the external controller via a hit line, thereby confirming that a
- 4 current instance of the search result.

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1 8. The circuit of claim 6, wherein said hash means is programmable to employ different 2 hash algorithms.

- 1 9. The circuit of claim 8, wherein said hash means includes a plurality of pre-programmed
- 2 hash algorithms, thereby permitting selectively employing a particular said hash algorithm.
- 10. 1 The circuit of claim 6, wherein said controller means is further for programming said
- 2 CAM means with new entries in said CAM database, thereby permitting programming to avoid
- 3 newly determined hash collisions.

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- 1 11. A method for searching an external memory containing search results by using a search 2 value received from an external controller, the method comprising the steps of:
 - (a) generating a hash output from the search value, wherein said hash value is smaller in size than the search value;
 - (b) comparing the search value against a CAM database of pre-stored instances of the search value known to cause hash collisions, wherein a CAM output is created if a match exists;
 - (c) creating an address value based on said CAM output if a said match exists and otherwise creating said address value based on said hash output, wherein said address value represents an address in the external memory; and
 - (d) providing said address value to the external memory, thereby permitting finding the search results in the external memory based on the search values.
- 1 12. A circuit to search an external memory containing search results based on a search value 2 received from an external controller, comprising:
 - a plurality of serially connected hash units each able to receive an input value and generate a hash value based there on, wherein said input value includes all or part of the search value or a said hash value of a prior said hash unit, and wherein the last said hash value is a hash output;
 - a plurality of CAM units equaling said hash units, whereby each respective said CAM unit is definable as having a paired said hash unit;
- said CAM units able to store a CAM database of instances of said input values known to 9 10 cause hash collisions in its paired said hash unit;

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| 11 | | said CAM units further able to receive a said input value common with its paired said | | | | | |
|----------------------------------|---|--|--|--|--|--|--|
| 12 | hash unit, to match said input value against its said CAM database, and to p | | | | | | |
| 13 | | a CAM output if a match exists; | | | | | |
| 14 | a logic unit able to receive said hash output and said CAM outputs and create an address | | | | | | |
| 15 | value based there on, wherein said address value represents an address in the | | | | | | |
| 16 | external memory; and | | | | | | |
| 17 | said logic unit further able to provide said address value on an output bus connecting the | | | | | | |
| 18 | circuit to the external memory, thereby permitting finding the search results in | | | | | | |
| 19 | | external memory. | | | | | |
| 5 1 | 13. | The circuit of claim 12, wherein said hash unit is programmable to employ different hash | | | | | |
| 01 02 10 10 10 10 | algorithms. | | | | | | |
| 됩 네 1 | 14. | The circuit of claim 13, wherein said hash unit includes a plurality of pre-programmed | | | | | |
| 切1 型 型2 | hash algorithms, thereby permitting selectively employing a particular said hash algorithm. | | | | | | |
| | | | | | | | |
| | 15. | The circuit of claim 12, wherein said CAM unit is programmable with new entries for | | | | | |
| 口 山 ² | said CAM database, from the external controller, thereby permitting the external controller to | | | | | | |
| | progr | program the circuit to avoid new hash collisions. | | | | | |
| 1 | 16. | The circuit of claim 12, further comprising: | | | | | |
| 2 | | a plurality of hash input logics, one per said hash unit, selectively able to route said input | | | | | |
| 3 | | values to their respective said hash units and to said CAM units; | | | | | |
| 4 | | a CAM input logic able to selectively route said input values to said plurality of CAM | | | | | |
| 5 | | units; and | | | | | |
| 6 | | a CAM output logic able to selectively combine said CAM outputs, thereby permitting | | | | | |
| 7 | | configurable application of said pluralities of said hash units and said CAM units. | | | | | |
| 1 | 17. | The circuit of claim 12, wherein said logic unit is further able to create one or more hash | | | | | |
| 2 | addresses based on said hash output and an offset value, and to additionally permit creating sa | | | | | | |

address value based on a pointer value and a hash hit signal, and the circuit further comprising:

a search data storage able to store a plurality of hash pointer values and a plurality of 4 5 search data values, wherein said hash pointer values represent potential instances 6 of said hash outputs and said search data values represent potential instances of 7 said search values; 8 said search data storage further able to receive said hash address from said logic unit, to 9 retrieve a said hash pointer value based on said hash address, to provide said hash 10 pointer value to said logic unit as said pointer value, and to retrieve a said search 11 data value based on said hash pointer value; and 12 a comparator operationally connected to said input bus, said comparator able to receive 13 the search value from said input bus, to receive said search data value from said search data storage, to compare the search value and said search data value to determine whether a match exists, and, if a said match exists, to provide said hash hit signal to said logic unit, thereby permitting the external memory to not store any instances of the search values. The circuit of claim 17, wherein said logic unit is further able to generate a search hit 18. □₂ □3 signal based on said hash hit signal and whether a said match exists in said CAM unit, and to provide said search hit signal to the external controller via a hit line, thereby confirming that a **⊕**4 current instance of the search result. ᆜ 19. The circuit of claim 17, further comprising: 1 2 a plurality of hash input logics, one per said hash unit, selectively able to route said input 3 values to their respective said hash units and to said CAM units; 4 a CAM input logic able to selectively route said input values to said plurality of CAM 5 units; and

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20. A circuit for searching an external memory containing search results based on a search value received from an external controller, comprising:

a CAM output logic able to selectively combine said CAM outputs, thereby permitting

configurable application of said pluralities of said hash units and said CAM units.

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a plurality of serially connected hash means for each receiving an input value and generating a hash value based there on, wherein the first said hash means operationally connects to input bus means for connecting the circuit to the external controller and wherein said input value includes all or part of the search value or a said hash value of a prior said hash unit, and wherein the last said hash value is a hash output;

- a plurality of CAM means, equaling said hash means, whereby each respective said CAM means is definable as having a paired said hash mean;
- said CAM means for storing a CAM database of instances of said input values known to cause hash collisions in its paired said hash means;
- said CAM means further for receiving a said input value common with its paired said hash means, for matching said input value against its said CAM database, and for providing a CAM output if a match exists;
- logic means for receiving said hash output and said CAM outputs and for creating an address value based there on, wherein said address value represents an address in the external memory; and
- said logic means further for providing said address value on output bus means for connecting the circuit to the external memory, thereby permitting finding the search results in the external memory.
- 1 21. The circuit of claim 20, wherein said hash means is programmable to employ different
- 2 hash algorithms.
- 1 22. The circuit of claim 21, wherein said hash means includes a plurality of pre-programmed
- 2 hash algorithms, thereby permitting selectively employing a particular said hash algorithm.
- 1 23. The circuit of claim 20, wherein said controller means is further for programming said
- 2 CAM means with new entries in said CAM database, thereby permitting programming to avoid
- 3 newly determined hash collisions.
- 1 24. The circuit of claim 20, further comprising:

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current instance of the search result.

| 2 | a plurality of hash input logic means, one per said hash means, for selectively routing | | | | |
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| 3 | said input values to their respective said hash means and to said CAM means; | | | | |
| 4 | CAM input logic means for selectively routing said input values to said plurality of CAM | | | | |
| 5 | means; and | | | | |
| 6 | CAM output logic means for selectively combining said CAM outputs, thereby | | | | |
| 7 | permitting configurable application of said pluralities of said hash means and said | | | | |
| 8 | CAM means. | | | | |
| 1 | 25. The circuit of claim 20, wherein said logic means is further for creating one or more hash | | | | |
| _ 2 | addresses based on said hash output and an offset value, and for additionally permitting creating | | | | |
| 급 급3 | said address value based on a pointer value and a hash hit signal, and the circuit further | | | | |
| 口 ①3 ①4 几 以5 | comprising: | | | | |
| ≒ું5 | search data storage means for storing a plurality of hash pointer values and a plurality of | | | | |
| | search data values, wherein said hash pointer values represent potential instances | | | | |
| ₫7 | of said hash outputs and said search data values represent potential instances of | | | | |
| 8 | said search values; | | | | |
| 38 119 110 111 | said search data storage means further for receiving said hash address from said logic | | | | |
| <u>1</u> 0 | means, for retrieving a said hash pointer value based on said hash address, for | | | | |
| | providing said hash pointer value to said logic means as said pointer value, and | | | | |
| 12 | for retrieving a said search data value based on said hash pointer value; and | | | | |
| 13 | said comparator means for operationally connecting to said input bus means, for | | | | |
| 14 | receiving the search value from said input bus means, for receiving said search | | | | |
| 15 | data value from said search data storage means, for comparing the search value | | | | |
| 16 | and said search data value to determine whether a match exists, and, if a said | | | | |
| 17 | match exists, for providing said hash hit signal to said logic means, thereby | | | | |
| 18 | permitting the external memory to not store any instances of the search values. | | | | |
| 1 | 26. The circuit of claim 25, wherein said logic means is further for generating a search hit | | | | |
| 2 | signal based on said hash hit signal and whether a said match exists in said CAM means, and to | | | | |

provide said search hit signal to the external controller via a hit line, thereby confirming that a

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| 1 | 27. | The circuit of claim 25, further comprising: |
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| 2 | | a plurality of hash input logic means, one per said hash means, for selectively routing |
| 3 | | said input values to their respective said hash means and to said CAM means; |
| 4 | | CAM input logic means for selectively routing said input values to said plurality of CAM |
| 5 | | means; and |
| 6 | | CAM output logic means for selectively combining said CAM outputs, thereby |
| 7 | | permitting configurable application of said pluralities of said hash means and said |
| 8 | | CAM means. |
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| ⊒1 | 28. | A method for searching an external memory containing search results based on a search |
| □ ¹ □2 □ 103 | value | received from an external controller, the method comprising the steps of: |
| TJ3 | | (a) generating a plurality of hash outputs based on respective input values having |

- (a) generating a plurality of hash outputs based on respective input values having decreasing order, wherein said input values include all or part of the search value or a said input value of just higher order;
- (b) comparing said respective input values against a like number of respective CAM databases such that respective CAM outputs are created if respective matches exist, wherein said respective CAM databases include pre-stored instances of said input values known to cause hash collisions;
- (c) creating an address value based on said CAM output produced responsive to the highest order said input value producing a said match, if any, and otherwise creating said address value based on the last said hash output, wherein said address value represents an address in the external memory; and
- (d) providing said address value to the external memory, thereby permitting finding the search results in the external memory based on the search values.